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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/390,079	09/03/1999	DARREN KERR	112025-0167	6305

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EXAMINER
ELLIS, RICHARD L

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

--The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address--

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE <u>3 (Three)</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on <u>5/21/2002 and 8/13/2002.</u>

☒ This action is FINAL

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) <u>1-37.</u> is/are pending in the application.

☐ Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) <u>1-37.</u> is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

    ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

    ☐ received

    ☐ received in Application No. (Series Code/Serial Number) _____.

    ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

      *Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

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Office Action Summary

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1.　　　　Claims 1-21 remain for examination. Claims 22-37 are newly presented for examination.

2.　　　　The numbering of claims is not accordance with 37 CFR § 1.126. The original numbering of the claims must be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When claims are added, except when presented in accordance with 37 CFR § 1.121(b), they must be renumbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 20-35 have been renumbered 22-37, respectively.

3.　　　　Claims 29-35 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A)　　The following terms lack proper antecedent basis:

1.　　"said first and second input registers" claims 30, 31;

2.　　"said first input register" claim 32;

B)　　The scope of meaning of the following claims are unclear:

1.　　The scope of claims 36 and 37 is unclear. It is unclear if applicant intends to provide an independent claim, or if applicant means to provide a dependent claim. In the case where applicant intends for claims 36 and 37 to be independent, then both claims 36 and 37 are incomplete in that they omit significant structural elements (in fact, all structural elements) of the invention. See MPEP § 2172.01.

4.　　　　Claims 36 and 37 are rejected under 35 USC § 112, fourth paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim. In the situation where applicant intended claims 36 and 37 to be dependent claims, then the claims fail to further limit the claimed system set fourth in their parent claims because the claims do not set fourth any additional structural elements or functionality of the system set forth in the parent claims. In fact, all the claims state is that the identical system to the parent claim is

packaged into different containers. But placing a device X into a container Y or a container Z, where containers Y and Z are wholly unrelated to device X (as is the case with these claims) does not limit device X in any way, shape, or form.

5.   The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

6.   Claims 1-21 are rejected under 35 USC 102(e) as being clearly anticipated by Asato, U.S. Patent 6,145,074.

        Asato was cited as a prior art reference in paper number 4, mailed August 13, 2002.

7.   The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 4, mailed August 13, 2002.

8.   New claims 22-35 are rejected under 35 USC 102(e) as being clearly anticipated by Asato, U.S. Patent 6,145,074.

9.   As to new claim 22, Asato taught a processor (fig. 4) comprising

        an execution unit (2) having an input (part of box 2 connected to input registers 3, 4) and an output (10, 13);

        an input register (3, 4) connected to said input and said output (fig. 2, 3, 4, 10, 5, 6) of said execution unit; and,

        a register decode value (s1, s2) that specifies bypassing data from said output of said execution unit (10) to said input register during a write back cycle transferring data to a register file (1) (col. 5 lines 50-52, col. 6 lines 15-32).

10.   As to claim 23, Asato taught a first instruction having at least one source operand and a first destination operand (fig. 3);

        a second instruction having at least one second source operand and a second destination operand (fig. 3), said at least one source operand is the same as said first destination operand (col. 1 lines 40-45, col. 2 lines 10-14, col. 3 lines 11-22); and,

        means for replacing said at least one second source operand with said register decode value (col. 2 line 65 to col. 3 line 12).

11.	As to claim 24, Asato taught means for loading said at least one first operand from said register file (fig. 4, 11, 12).

12.	As to claim 25, Asato taught means for loading the at least one first source operand from a memory (col. 9 lines 15-18).

13.	As to claim 26, Asato must inherently have had an instruction decode mechanism within the system disclosed.

14.	As to claim 27, the register decode value must inherently have fewer bits than the source operand, because to do otherwise (have the register decode value have the same number of bits as the source operand) would mean there would be no need for register decode values because the source operand could be fully specified within the instruction word itself.

15.	As to claim 28, Asato taught a first execution unit (fig. 6, 21-1) having at least one first input and a first output (inherent);

at least one second execution unit (21-2) having at least one second input and a second output (inherent);

a first input register connected to said at least one first input (fig. 2, fig. 4, col. 6 lines 50-53);

a second input register (fig. 2, fig. 4, col. 6 lines 50-53)

a multiplexer (fig. 7) having a first input from said first input register (col. 7 lines 3-4), a second input from said second input register (col. 7 lines 3-4), and an output to said at least one second execution unit (72, 73); and,

a register decode value that specifies bypassing data from said first input register to said at least one second execution unit via said multiplexer (col. 7 lines 5-8).

16.	As to claim 29, Asato taught a first instruction (fig. 3, fig. 5) having at least one first source operand (s1, s2) and a first destination (dst), said first execution unit processing said first instruction (inherent because if the execution units do not process the instructions, no useful work is performed by the processor);

a second instruction (fig. 3, fig. 5) having at least one second source operand (s1, s2)

and a second destination (dst) operand, said at least one second source operand is the same as said at least one first source operand (this is conventionally known as a read dependency);

means for replacing said at least one second source operand with said register decode value (col. 7 lines 5-8, in order for control to be implemented using only s1 and s2 fields, a means must be present to insert the proper values into the s1 and s2 fields of the instructions for the system to function).

17.   As to claim 30, Asato taught a register file (fig. 2, 1, fig. 4, 1) connected to said first and second input registers (col. 7 lines 3-5); and,

means for loading said at least one first and said at least one second source operands from said register file (fig. 2, 14, 15, 12, 11, fig. 4, 14, 15, 12, 11).

18.   As to claim 31, Asato taught a memory connected to said first and second input registers (col. 9 lines 16-18); and,

means for loading said at least one first and said at least one second source operands from said memory (col. 9 lines 16-18, in order to process a load, the system must inherently load data from memory).

19.   As to claim 32, Asato taught an instruction decode mechanism (must be inherently present);

means for said multiplexer choosing input from said first register (fig. 4, 16, 17).

20.   As to claim 33, Asato taught the register decode value must inherently have fewer bits than the source operand, because to do otherwise (have the register decode value have the same number of bits as the source operand) would mean there would be no need for register decode values because the source operand could be fully specified within the instruction word itself.

21.   As to claims 34 and 35, Asato taught a displacement value (col. 9 lines 23-27) within said at least one first and said at least one second source operands, the displacement value specifying an effective memory address where data is stored (col. 8 lines 13-38).

22.   New claims 36 and 37 are rejected under 35 USC § 103 as being unpatentable over

Asato, as applied to claim 9, <u>supra</u>.

As to claims 36 and 37, Asato did not per se. claim a set of instructions on a computer readable media or information embodied within electromagnetic waves propagating over a computer network for performing the disclosed system. However, Asato clearly disclosed instructions and information (col. 1 line 15 to col. 2 line 46). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have stored those instructions or information on computer readable media, as well as to have propagated that information over a network in the form of electromagnetic waves <u>because</u> in order for a computer to perform in Asato disclosed manner, it must receive instructions or information for doing so, and as those instructions or information do not spontaneously appear within the computer from nowhere, they must therefore have been introduced via either a medium readable by the computer, or by propagating electromagnetic waves over a network to the computer.

23.   Applicant's arguments filed May 21, 2002 and September 9, 2002, paper numbers 8 and 11, have been fully considered but they are not deemed to be persuasive.

24.   In the remarks, applicant argues in substance:

A)   That: "Asato does not show applicants' claimed novel *'the instruction set defining a register decode value, that specifies one of a first register decode value which defines source operand bypassing, and a second register decode value that defines result bypassing from a previous instruction executing in pipeline stages of the processor'*" (emphasis unchanged, paper 8, pg. 8)

This is not found persuasive because to the extent with which this aspect has been amended into applicant's claims, Asato continues to anticipate this concept. First, Asato taught "register decode values" which specify one of a "first register decode value which defines source operand bypassing" and "a second register decode value that defines result bypassing from a previous instruction executing in pipeline stages of the processor" at least at fig. 4, elements s1, s2, 16, and 17, and at col. 6 lines 7-14). Additionally, Asato taught that these values are used to determine source operand bypassing, or result bypassing, depending upon the particular values themselves (col. 6 lines 15-31).

B)   That: "In some embodiments, Asato has dedicated software that determines the dependencies between several consecutive instructions, and then determines the values of logical values that determine switches of multiplexers. In sharp contrast, Applicants' invention is concerned with selection of a correct register decode value rather than computing logical values. For this reason, Applicants do not have the aforementioned software or additional logic that Asato teaches, because, as shown in Applicants' specification, they have become unnecessary in Applicants' device." (paper 8, pg. 9)

This is not found persuasive because applicant's argument is wholly irrelevant to the fact that, to the extent claimed, Asato anticipates the claimed features of applicant's invention. The fact that Asato may or may not contain additional software that calculates the logical values used by his bypassing network has no bearing upon the reading of Asato upon Applicant's claims, because applicant's claims begin with the term "comprising".

> "The term comprises is inclusive and fails to exclude unrecited steps. In re Horvitz, 168 F 2d 522, 78 USPQ 79 (CCPA 1948). The use of the term comprising to introduce the claimed structure means that the device covered by those claims may involve many more elements than those positively recited. Ex parte Gottzein et al.. 168 USPQ 176 (PTO Bd. App. 1969). Comprising leaves the claim open for the inclusion of unspecified ingredients even in major amounts. Ex parte Davis et al., 80 USPQ 448 (PTO Bd. App. 1948)."

Accordingly, the fact that Asato may or may not disclose additional elements or steps beyond that which applicant has claimed is immaterial as to whether Asato has disclosed those steps that applicant has claimed. As Asato discloses Applicant's claimed elements and steps, Asato anticipates Applicant's claim.

C)   That: "Asato does not show applicants' claimed novel *'a register decode value that specifies bypassing data from said output of said execution unit to said input register during a write back cycle transferring said data to a register file'*. Applicant's processor uses bypass determined by using different register decode values for different source operands. Applicant uses *a register decode value that specifies bypassing data from said output of said execution unit to said input register during a write back cycle transferring said data to a register file*." (paper 11, pg. 3)

This is not found persuasive because as has been pointed out, supra., Asato does indeed teach a register decode value that specifies bypassing (fig. 3, s1, s2, fig. 4, s1, s2, col. 6 lines 7-14). Additionally, as seen from fig. 4, the bypassing taught by Asato is of an output of an execution unit (2, 10) to an input register (3, 4) during a writeback cycle (col. 5 lines 50-52).

25.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a). The practice of automatically extending the

shortened statutory period an additional month upon the filing of a timely first response to a

final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

26.   Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
November 14, 2002

Richard Ellis
Primary Examiner
Art Unit 2183